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Cryogenic shallow reactive ion etch process on silicon on insulator

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Deep RIE etching of silicon has been previously investigated particularly with respect to etch rate, etch profile and selectivity. While using an oxide layer as an etch stop has also been investigated, the profile control near the oxide interface is usually not very important due to the large aspect ratios. However for shallow structures with low aspect ratios, such as shallow 2-D photonic crystal type dense pattern microstructures (usually with thickness less than 500nm and with low aspect ratios ~1-4) on a Silicon On Insulator (SOI) platform, profile control near the oxide interface is important while the etch rate and the selectivity are not as much of a concern. We show how the presence of an insulating layer close to the silicon etch surface makes the cryogenic etch process different from that of bulk silicon in many respects.

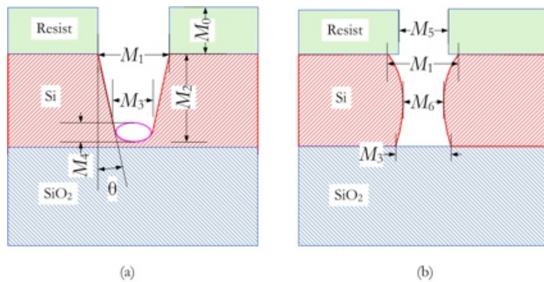

Figure 1, The shallow etch profile a) before and b) after reaching the oxide etch stop layer with parameters for measurement defined.

Selecting a set of parameters as a base line and defining some geometrical parameters to characterize the etch profile enabled us to study the effect of various etch parameters systematically by varying them one at a time around the base line [1,2] (see Fig. 1). We investigated the RIE lag phenomena where we observed that the RIE lag is affected by extra charging due to the presence of an insulating layer near the etch region. We have shown that the charging effect is dominant only when etching approaches the BOX layer. This may explain why notching appears when we continue etching after reaching to the BOX layer. A simple 1-D model has been used to predict the temperature difference from the clamp to the top silicon layer and the ambiguity at the top silicon layer based on the ambiguity on the grease layer thickness. We have shown that the temperature difference can be as large as $1.5\pm0.5^{\circ}C$ provided the grease thickness varies as $60\pm20\mu m$. We observe that at very low temperatures of $-135°C$, the preferential etching of silicon becomes important. The selected base line parameters has a relatively low ICP power that is not enough to ionize all etching agents, so at very low chamber pressure, grass starts to grow. The effect of varying the CCP has also been considered. We have shown that there is higher potential barrier for the incoming ions than the bulk silicon case (based on our simple model it is 16.8 times higher). It means that for etching silicon on the SOI wafers we need more CCP power than the bulk silicon. We observed that at very low pressure, and due to low ICP, grass tends to grow. The effects of oxygen flow rate on etching have also been considered. We observed that preferential etching of silicon can happen at very low oxygen flow rate. We show how notches and footings are a function of etch time and so a precise choice of etch time is critical for obtaining a good etch profile in SOI wafers (see Fig.2) [2].

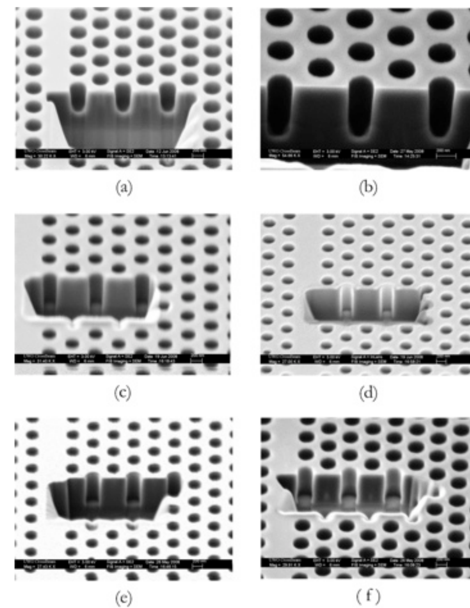

Figure 2. SEM micrograph image of the etch profile using the baseline parameters after a) 3min, b) 4 min, c) 5min, d) 5.5 min, e) 6 min and f) 7min of etching .

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References

1. Pruessner, M. W., Rabinovich, W. S., Stievater, T. H., Park, D., and Baldwin, J. W., J. Vac. Sci. Technol. B 25(1), 21 (2007).
2. Aref Bakhtazad, Xuan Huo, and Jayshri Sabarinathan, J. Vac. Sci. Technol. B 29, 041001 (2011).

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